REMARKS

In the Final Official Action, the Examiner rejected all pending claims 1-12 and objected to the drawings. Applicants respectfully traverse the rejection of the claims 1-12. In addition, Applicants have submitted a set of replacement drawings. Reconsideration of the Application in view of the remarks set forth below is respectfully requested.

Objections to the Drawings

On the Summary page of the Official Action, the Examiner objected to the drawings. However, the Examiner did not provide any specific comments with regard to the objection. In the present response, Applicants have provided replacement drawing sheets of Figures 1-4, which are attached hereto as Appendix A and are each identified as a "Replacement Sheet." The replacement drawing sheets are believed to overcome the Examiner's objection by providing a clean copy of the drawings. Accordingly, Applicants respectfully request withdrawal of the Examiner's objection to the drawings.

First Rejection Under 35 U.S.C. § 103

The Examiner rejected claims 1-12 under 35 U.S.C. § 103(a) as being rendered obvious by McAdams (U.S. Patent No. 5,301,160) in view of Weaver et al. (U.S. Patent No. 4,107,596). However, in the detailed discussion of the rejection as applied to the claims, the Examiner only discussed the reference as applied to claims 1-6 and 8-11. Further, the Examiner admitted in another rejection, which is discussed below, that the McAdams and Weaver references failed to disclose various features recited in claims 7 and 12. Accordingly, Applicants believe that the Examiner inadvertently stated that each of claims 1-12 is rejected by these combined references

and that claims 1-6 and 8-11 are the only claims rejected under the proposed combination of the McAdams and the Weaver references. With regard to independent claim 1, the Examiner stated:

> Regarding **claim 1**, McAdams discloses a system comprising: a processor (fig. 1, 102), a power supply coupled to the processor (fig. 1, 112); and a device coupled to the processor and the power supply and comprising (fig. 2): an internal power supply bus configured to receive a power signal from the power supply (fig. 2, buses internal to 145 supplying Vdd 112); and an isolation circuit configured to disconnect the internal power supply bus from the power supply bus by interrupting the flow of the power signal (fig. 2, isolating circuit being p-mos transistors 282 and 284, which are configured to interrupt the power signals to TL and TR lines, which feed power to the memory section, right dotted box in fig. 2).
> Although McAdams did not explicitly show the isolation circuit receives a control signal to interrupt the flow of power during a standby mode; however practice of such feature, in which standby signal which control the isolation circuit to isolate the power from the load, is considered well known in the art. An exemplary instance is shown by Weaver et al. (col. 10, lines 57-60, '...OFF high impedance state for the duration of the standby mode in response to the standby-operate signal for isolating the load from the battery...').
> Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to combine the teaching by Weaver to the disclosure of McAdams so that minimal control current during standby mode (col. 1, lines 35-42).

Applicants respectfully traverse this rejection. The burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (PTO Bd. App. 1979). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Accordingly, to establish a *prima facie* case, the Examiner must not only show that the combination includes *all* of the

claimed elements, but also a convincing line of reason as to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the teachings of the references. *Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I. 1985). When prior art references require a selected combination to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gained from the invention itself, i.e., something in the prior art as a whole must suggest the desirability, and thus the obviousness, of making the combination. *Uniroyal Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 5 U.S.P.Q.2d 1434 (Fed. Cir. 1988).

The present application is directed to a technique for implementing a zero power standby mode with reduced leakage current. In operating electronic devices, a standby mode or a sleep state is typically implemented to maintain power to certain components when the system is not in use. Typical electronic devices lose some leakage current even though they are in a standby mode or a sleep state. *See* Application, p. 3, lines 15-22. To prevent or further reduce the leakage currents in the standby mode, an isolation circuit in accordance with the present invention may be implemented. *See* Application, p. 6, line 21-p. 7, line 3. The isolation circuit, which may be activated by a control signal, may be used to disconnect an internal power supply bus from an external voltage source to reduce leakage currents in response to initiating a standby mode. *See* Application, p. 9, lines 3-9; p. 9, lines 15-27; p. 10, line 25 – p. 11, line 7. Specifically, claim 1 recites "an isolation circuit configured to disconnect the internal power supply bus from the power supply by interrupting the flow of the power signal when a standby mode is indicated by a control signal received at the isolation circuit."

In contrast, the McAdams reference discloses a selection circuit that enables transmissions through transfer gates *in response to address signals*. *See* McAdams, col. 2, lines 31-32. The selection circuit provides either a pre-charged voltage to the transfer gates or a high level signal to one of the transfer gates when selecting a transfer gate. *See* McAdams, col. 2, lines 33-36. In the McAdams reference, the bitline isolation control circuit 145 switches between a pre-charged state and an active state depending on the row address select signals RA8 and $\overline{RA8}$ along with the row address selection signals RA9 and $\overline{RA9}$, which are applied to the inputs of the bitline isolation control circuit 145. *See* McAdams, col. 5, lines 26-47. These signals are provided to the bit isolation control circuit 145 from the row address decoder 124. *See* McAdams, col. 5, lines 15-17. Based on these signals, the transfer control leads TR and TL are coupled to an on-chip voltage supply Vpp or an off-chip voltage supply Vdd. *See* McAdams, col. 5, lines 40-55. The only signals to be received by the bit line isolation control circuit 145 are these address signals that are utilized to provide specific memory bitlines to the sense amplifier 200 through the transfer control leads TR and TL. *See* McAdams, Fig. 2; col. 5, lines 21-32.

The Weaver reference is directed to a bidirectional DC-to-DC power converter. *See* Weaver et al., col. 1, lines 7-10. In the Weaver reference, a handheld unit 110 is separable into a control module 130 and a power module 140. *See* Weaver et al., col. 2, lines 31-32. The power module 140 contains a power source 142 and a power control logic 144 that provides a low power standby mode when the control module 130 is not active. *See* Weaver et al., col. 2, lines 37-41. A standby voltage V_{SBY} is applied throughout the unit 110 to maintain the standby status, while an operate voltage V_{OPR} is utilized to activate the device and control circuits. *See* Weaver et al., col. 2, lines 41-45. The power source 142 includes a power supply 220 along with a

battery 204. *See* Weaver et al., Fig. 2, col. 2, lines 62-67; col. 3, lines 14-32. As part of the elements of the power supply 220, transistors Q1, Q2 and Q3 operate with a ramp generator 516 and a feedback amplifier 520. *See* Weaver et al., col. 7, line 20 - col. 8, line 43. As such, the bidirectional power converter of the Weaver reference is a portion of the power supply or power converter 220.

In the rejection of claim 1, the Examiner asserted that the bitline isolation control circuit 145 is equivalent to the "device," that the enhancement mode MOS transistors 282 and 284 are equivalent to the "isolation circuit," and that the transfer control leads TR and TL are equivalent to the "internal power supply bus." Further, the Examiner admitted that the McAdams reference does not explicitly show that the isolation circuit receives a control signal to interrupt the flow of power during a standby mode. In an attempt to cure this deficiency, the Examiner appears to assert that it is "well-known" in the art to provide a "standby signal which control the isolation circuit to isolate the power from the load," and combines the Weaver reference with the McAdams reference to provide the missing recited feature.

However, Applicants assert that the McAdams reference and Weaver reference, even in combination, fail to render the claimed subject matter obvious for at least two reasons. First, the references fail to disclose "an isolation circuit configured to disconnect the internal power supply bus from the power supply by interrupting the flow of the power signal when a standby mode is indicated by a control signal received at the isolation circuit," as recited in claim 1. Second, the Examiner has failed to provide a convincing line of reasoning as to why one of ordinary skill in

the art would have found any motivation or suggestion to make such a combination. Hence, the McAdams and the Weaver references fail to render the claimed subject matter obvious.

With regard to the first point, the McAdams reference and Weaver reference fail to disclose or teach "an isolation circuit configured to disconnect the internal power supply bus from the power supply by interrupting the flow of the power signal when a standby mode is indicated by a control signal received at the isolation circuit," as recited in claim 1. Specifically, in the McAdams reference, row address select and selection signals RA8, RA9, $\overline{RA8}$ and $\overline{RA9}$ are used by the bitline isolation circuit 145 to select between two voltage supplies that are supplied to the transfer control leads TR and TL. *See* McAdams, col. 5, lines 26-32. The McAdams reference clearly describes that the voltage supply selection circuits are controlled by the signals produced from the row address decoder 124, and are not *a control signal that indicates a standby mode*. *See* McAdams, col. 5, lines 15-17. In fact, the row address select and selection signals RA8, RA9, $\overline{RA8}$ and $\overline{RA9}$ are specifically described as providing access to specific bitlines in the memory array 110 for the sense amplifier 200 through the transfer control leads TR and TL. *See* McAdams, col. 5, lines 21-32. Clearly, nothing in the reference suggests or teaches that the enhancement mode MOS transistors 282 and 284 are controlled a standby mode or in response to a standby mode. Accordingly, the McAdams reference does not disclose or teach the claimed subject matter.

The Weaver reference fails to cure the deficiencies of the McAdams reference because the McAdams reference also fails to disclose or teach "an isolation circuit configured to disconnect

the internal power supply bus from the power supply by interrupting the flow of the power signal when a standby mode is indicated by a control signal received at the isolation circuit," as recited in claim 1. In the Weaver reference, a controlled output switching means is a part of a bidirectional power converter. *See* Weaver et al., col. 10, lines 20-64. As noted above, the power converter is described in the reference as the power source or converter 220. *See* Weaver et al., col. 6, lines 62-67. The power converter 220 is part of (i.e. internal to) the power supply, and the Weaver reference merely discloses disabling the supply of power from the power supply to other components of the system that are external to the power supply. It does not disclose *an isolation circuit in a device coupled to the power supply and a processor*, which is "configured to disconnect the internal power supply bus from the power supply by interrupting the flow of the power signal when a standby mode is indicated by a control signal received at the isolation circuit," as recited in claim 1.

Because the Weaver reference and the McAdams reference, alone or in combination, fail to disclose or suggest all the recited features, the cited references fail to render the claimed subject matter obvious. For this reason alone, the Examiner has failed to establish a *prima facie* of obviousness.

To the second point, the Examiner has also failed to meet the required burden of articulating a motivation for the combination of the McAdams and Weaver references. Instead, the Examiner stated that:

> Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to combine the teaching by Weaver to the disclosure of McAdams so that minimal control current during standby mode (col. 1, lines 35-42).

This statement is nothing more than an unsupported assertion, not a convincing line of reasoning as to *why* one of skill in the art would combine the references.

The Federal Circuit recently overturned the Board, which had upheld an Examiner's rejection in a similar situation. In the case of *In re Lee*, 61 U.S.P.Q.2d 1430 (Fed. Cir. 2002), the Examiner rejected the applicant's claims under 35 U.S.C. § 103 without providing a convincing motivation to combine references. The Board subsequently affirmed the Examiner's rejection. In overturning the Board's decision, the Federal Circuit stated that:

> When patentability turns on the question of obviousness, the search for and analysis of the prior art includes evidence relevant to the finding of whether there is a teaching, motivation, or suggestion to select and combine the references relied on as evidence of obviousness. *See, e.g., McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 1351-52, 60 U.S.P.Q.2d 1001, 1008 (Fed. Cir. 2001) ("the central question is whether there is reason to combine [the] references," a question of fact drawing on the Graham factors).
>
> 'The factual inquiry whether to combine references must be thorough and searching.' *Id.* It must be based on *objective evidence of record.* This precedent has been reinforced in myriad decisions, and cannot be dispensed with. [citations omitted]. *In re Lee*, 61 U.S.P.Q.2d at 1433 (emphasis added).

The Examiner's statement regarding minimal control current during the standby mode is not a convincing line of reasoning as to *why* one of skill in the art would combine the references. Accordingly, the Examiner's unsupported assertion does not meet the evidentiary standard required for combining references under Section 103.

Indeed, the McAdams reference describes providing alternatives for efficiently boosting the voltage of the gate electrodes to a greater voltage than the off-chip voltage supply voltage Vdd and efficiently returning the voltage of the gate electrodes to the

precharge voltage Vdd with lower power and in smaller chip areas. *See* McAdams, col. 1, line 65 – col. 2, line 6. Specifically, the McAdams reference describes voltage supply selection circuits, which are controlled by the signals produced from the row address decoder 124. *See* McAdams, col. 5, lines 15-17. These signals are provided to access specific bitlines in the memory array 110 for the sense amplifier 200 through the transfer control leads TR and TL. *See* McAdams, col. 5, lines 21-32. The operation of the circuits is not even related to a standby mode, but is based on address signals.

In contrast to the McAdams reference, the Weaver reference teaches a power converter that provides a standby mode and an operate mode. *See* Weaver et al., col. 1, lines 7-10. The Weaver reference is not concerned with address signals or providing access to a memory array, because the reference is directed to DC-DC power converters. In fact, the reference describes a power converter that is more efficient and that is able to operate in standby and operate modes with minimal control current to change the mode of the converter. *See* Weaver et al., col. 1, lines 34-42. Clearly, the Weaver and the McAdams references are directed to completely different problems and do not provide or support a motivation or suggestion for the combination of the references. Thus, the claimed subject matter cannot be rendered obvious by the cited combination.

Because the references fail to disclose *all* of the recited features much less provide a motivation to combine the references in the manner recited, Applicants respectfully assert that the references fail to support a *prima facie* case of obviousness. As such, Applicants respectfully request withdrawal of the Examiner's rejection and allowance of claims 1-6 and 8-11.

Second Rejection Under 35 U.S.C. § 103

The Examiner rejected claims 7 and 12 under 35. U.S.C. § 103(a) as being unpatentable over McAdams (U.S. Pat. No. 5,301,160) in view of Weaver et al. (U.S. Patent No. 4,107,596) and Hoffman et al. (U.S. Pat. No. 5,117,129). Applicants respectfully traverse this rejection.

Claims 7 and 12 depend from independent claim 1 and are believed to be patentable based on this dependence, and further based on the additional subject matter separately recited in each of the claims. Applicants respectfully submit that the Hoffman reference does not cure the deficiencies of the McAdams and Weaver references.

In the rejection, the Examiner admitted that the McAdams and the Weaver references fail to disclose an isolation circuit coupled between a pad on the device configured to receive the power signal and the internal power supply bus, and an I/O pad and circuitry coupled between the output buffer and the I/O pad to tri-state the I/O pad, as recited in claims 7 and 12. The Examiner relied on the Hoffman reference to disclose these recited features. However, the Hoffman reference is directed to cold sparing of a full rail logic swing CMOS off-chip driver that presents high impedance to ground when power is not present. *See* Hoffman, col. 1, lines 36-39. Specifically, the reference describes a CMOS circuit that presents high impedance when the voltage V_{DD} is equal to ground. *See* Hoffman, col. 3, lines 1-5 and 37-56. In the Hoffman reference, the pad signal 150 is coupled to the I/O pad 152 through a circuit, which includes various transistors and logic devices. *See* Hoffman, Fig. 3A, col. 3, lines 25-30. The circuit,

which the Examiner appears to assert is equivalent to the isolation circuit, is not coupled to an *internal power supply bus,* as recited in the present claims. Accordingly, the Hoffman reference does not disclose the subject matter recited in claims 7 and 12. Further, the operation of the circuit is not based on a *control signal that indicates a standby-mode*, but rather is based on the voltage V_{DD}. *See*, Hoffman, col. 3, lines 36-56. As such, the Hoffman reference does not disclose an *isolation circuit* that disconnects *internal power supply bus* in response to a *control signal that indicates a standby mode*.

Furthermore, to provide support for the proposed combination of the references, the Examiner merely stated:

> Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to include the feature shown by Hoffman et al. to the disclosure of McAdams to provide stable drive to loads, col. 2, lines 30-38.)

The Examiner's statement regarding providing stable drive to loads is not a convincing line of reasoning at to *why* one of skill in the art would combine the references. Accordingly, the Examiner's unsupported assertion does not meet the evidentiary standard required for combining references under Section 103.

As noted above, the McAdams reference, the Weaver reference and the Hoffman reference simply do not provide a suggestion or motivation for the asserted combination. The McAdams reference is related to providing alternatives to efficiently boosting the voltage of the gate electrodes greater than the off-chip voltage supply voltage Vdd and returning the voltage of the gate electrodes to the precharge voltage Vdd for a memory device. In contrast, the Weaver

reference is not concerned with address signals or providing access to a memory array because the reference is directed to DC-DC power converters. Indeed, the reference describes a power converter that is more efficient and that is able to operate in a standby mode and operate mode with minimal control current to change the mode of the converter. *See* Weaver et al., col. 1, lines 34-42. Further, the Hoffman reference is directed to cold sparing of a full rail logic swing CMOS off-chip driver that presents high impedance to ground when power is not present. *See* Hoffman, col. 1, lines 36-39. As such, the references simply do not provide a suggestion or motivation for the asserted combination

Therefore, claims 7 and 12 are patentable by virtue of their dependency from independent claim 1 as well as the subject matter recited in each of the claims. Accordingly, Applicants respectfully request withdrawal of the rejection and allowance of claims 7 and 12.

Conclusion

In view of the remarks set forth above, Applicants respectfully request withdrawal of the Examiner's rejections and allowance of claims 1-12. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

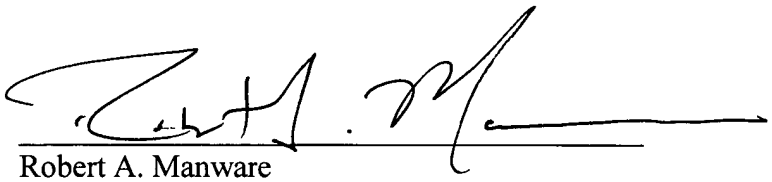
General Authorization for Extensions of Time

In accordance with 37 C.F.R. § 1.136, Applicants hereby provide a general authorization to treat this and any future reply requiring an extension of time as incorporating a request therefore.

Furthermore, Applicants authorize the Commissioner to charge the appropriate fee for any extension of time to Deposit Account No. 13-3092; Order No. MICS:0071/FLE (00-0901).

Respectfully submitted,

Date: March 22, 2004



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